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Efficient Microarchitecture Design for the Internet of Things (IoT)-Edge Computing: A Review

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Abstract: Power consumption and resource utilization are important factors to be considered at the edge level of the Internet of Things (IoT) architecture. However, the microarchitecture design for the IoT-edge computing should be optimized and the aim of current paper is to review the microarchitecture optimization and computing paradigms for the IoT domain. Additionally, a proposed reconfigurable microarchitecture design is introduced and one of the microprocessor computing paradigms is employed that is the reconfigurable pipeline stages based on input pulses frequency from an external sensor to ensure the efficiency of the utilized resources and hence the consumed power at the IoT-edge level. The current research focuses on illustrating the benefits of designing an appropriate microarchitecture for IoT computing utilization as a step toward developing the next-generation IoT-microprocessors architectures.

Keywords: Microprocessor, Internet of Things (IoT), Microarchitecture, Edge Computing, Reconfigurability.

1 Introduction

Nowadays, most of gadgets around us have sensors attached to them and integrated with the internet, for example, smart watches can track our movements, measure our health indexes and send them via an application. Another example that shows the benefits of the internet of things (IoT) is the remedies suggested by the modern automobiles according to the driving situations. In addition to that, most of the industrial processes are integrated with digital technologies and form the 4th industrial revolution (industry 4.0) which characteristic by the industrial internet of things (IIoT) [1]. Industrial IoT (IIoT) is a result of integrating the actuators in the industry with internet connectivity for the aim of observations or control. For the closed-loop control, the feedback sensor readings are the essential stage to complete the controller loop. The device microprocessor is the main element in any controller implementation platform. Development of the microprocessors enables them to act as a core of IoT platforms starting from the nodes, then the gateways, and finally the servers. New microprocessors design requirements arise with the- state-of-the-art IoT, especially for edge nodes. However, the device microprocessor is the key element inside the digital boards that organize the data acquisition, the data processing and the internet connectivity for both IoT and IIoT architectures domains. So the microarchitecture design plays an important factor and hence the aim of current paper is to review this microarchitecture optimization and computing paradigms in the mentioned domains. Additionally, a reconfigurable microarchitecture design is proposed due to its importance in the frequency measurement of incoming pulses train from an external sensor which has wide rang applications in the industry [2]. This paper is organized as follows: section two includes the literature review related to the microarchitecture optimization for the IoT, a proposed reconfigurable computing system based on the pipelines stages is explained in section three, and, finally, the paper is concluded in section four.

2 Optimization of the Microarchitecture for IoT

Devices microprocessors, microcontrollers, and Field Programmable Gate Arrays (FPGA) play the

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core rule at the Internet of Things edge level and it should be right-provisioned. However, performing the computations at the edge stage reduces latency times, energy overhead problem, and communication bandwidth bottlenecks. Because the IoT is the new name of recent embedded systems, current fixed embedded systems architecture is no more efficient for IoT- Edge computing purposes due to power consumption and resource utilization constraints especially with the increased number of connected objects to the internet network. On another hand, many research articles in the IoT field recommended the utilization of the reconfigurable microarchitecture at the IoT edge level and recognize it as a research direction. In order to support the IoT growth, IoT microprocessors should have five key characteristics [3]. First key is efficiency; there are several resource constraints of IoT devices, so IoT microprocessors should be optimized for cost, energy, area and performance efficiency. Second key is configurability, several IoT applications require different runtime requirements, and this necessitates configurable/adaptable microarchitectures for next-generation IoT microprocessors in order to obtain optimal execution and thus optimal power consumption. Third key is security; it is a primary design goal because IoT microprocessors will be more susceptible to attacks. Fourth key is future-proof, future applications are to be executed with IoT microprocessor without being over-provisioned for current applications. Finally, fifth key is extensibility; extending the IoT microprocessors with additional functionalities will ensure its future proofing.

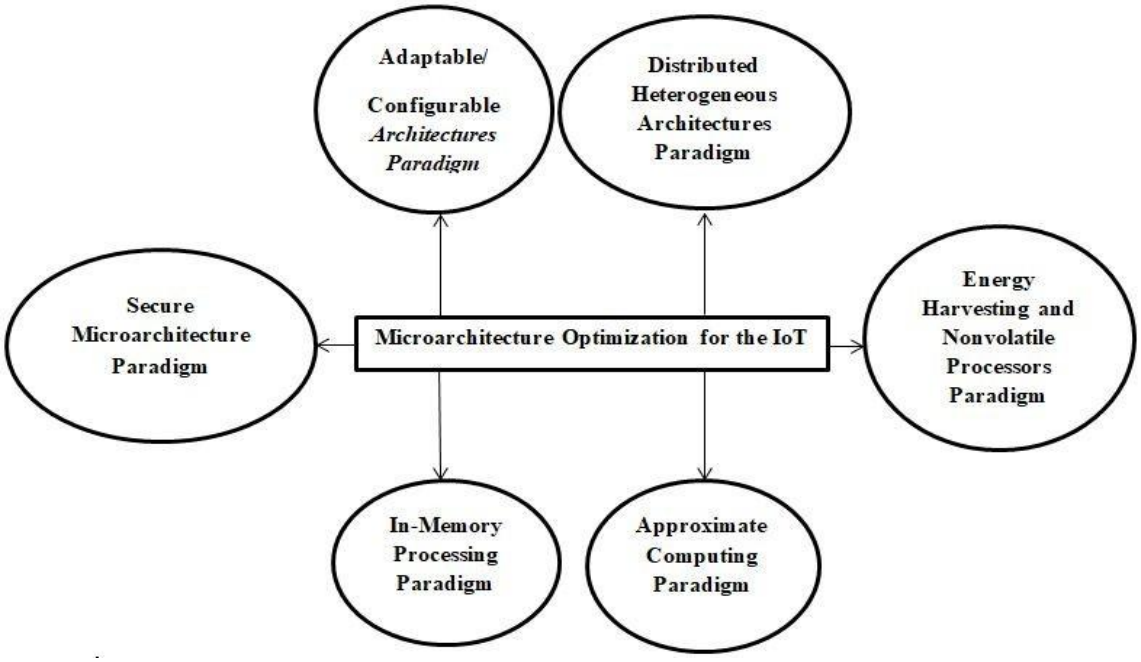

Figure 1: Microarchitecture optimization for the IoT.

In the following subsections, a few potential microprocessors optimizations and computing paradigms are served [3]. However, the reviewed microarchitecture optimization and computing paradigms for the IoT are illustrated in figure 1.

2.1 Adaptable/Configurable Architectures Paradigm

Adaptability/Configurability is obtained by the ability to change the microprocessor's configuration at runtime. This will insure the balance between power, area and performance in different IoT

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applications. For this reason, the next-generation IoT-microprocessors should be designed with adaptable/configurable architectures. There are many components in the microprocessor that can be configured and they are: pipelines [12], reorder buffer [13], issue queue [14], and register file [15]. Configurable caches [16] have potential effect on the microprocessor's end-to-end area, energy and power.

2.2 Distributed Heterogeneous Architectures Paradigm

Heterogeneous architectures contain different cores with different performance and capabilities which can execute the same instruction set. The software of the concern application will determine the core that best ensures the optimization behavior based on evaluating the resources requirements [17]. DSPs, CPUs and GPUs are the heterogeneous architectures cores. The benefit here is that: existing cores can be reutilized in the designing of heterogeneous microprocessors; this enable prior design and verification works to be done. More efforts and time are required in order to obtain a reduced design space with the heterogeneous architectures. However, if the number of applications is increased, then heterogeneous architectures may provide less optimization potential than adaptable architectures. The number and choice of the cores is a major challenge and scheduling of applications to the best core is another major challenge in designing the heterogeneous architectures for the IoT [4] [18]. A priori knowledge and analysis of applications domains are required to obtain a suitable platform that ensure the execution requirements. The distributed heterogeneous architectures in the form of a network are an alternative to heterogeneous cores on one device. The challenges in utilizing distributed heterogeneous architectures are: transmission and execution times, energy constraints and the benefit of waiting for right-provisioned node if it is busy.

2.3 Energy Harvesting and Nonvolatile Processors Paradigm

Energy consumption is one of the most important challenges for IoT devices. Power sources (like batteries) are to be replaced by energy harvesting techniques. Radio frequency radiation, solar and thermal gradients are sources for energy harvesting [5] [19-22]. Due to the external effects (e.g. electromagnetic signals, distance from an energy source and physical obstacles) those energy sources are unreliability [23], thus if the system is equipped with energy harvesting, then the traditional processors (volatile processors) will be impractical as they will lose their operating state when the power supply is disrupted. The solution with this case is nonvolatile processors as they use nonvolatile memories to save the processor state when the energy source is disrupted [24]. With nonvolatile components, the processor will continue the execution from the nonvolatile memory once the power is restored. Another important point is that: as most embedded systems have valuable idle state, the nonvolatile processors will make the system shut down in idle state resulting in power harvesting [25] [26]. Several ReRAMs, PCRAMs, STTRAMs and FeRAMs have been developed for the use in power harvesting systems [6] [24] [27-29]. Both application and input power characteristics [30] affect the choice of nonvolatile architectures.

2.4 Approximate Computing Paradigm

Even approximate computing gives an inaccurate result, but this result maintains the required output quality [31], so a lot of traction is gained to use it as alternative to exact computing. With approximate computing, new optimization options are allowed for processors that perform execution for flexible applications. Power-efficient edge computing can be enabled using approximate computing in IoT devices, like wearable electronics [7] [32]. Identifying both device's application

and application's flexibility to computing error is the first step to include approximate computing in IoT devices. At the circuit level, many techniques for obtaining inexactness have been proposed [33] using different approximate components, for examples: approximate logic synthesis [34] [35], approximate adders [8] [37] and approximate multipliers [38] [39].

2.5 In-Memory Processing Paradigm

Without the need for processor-to-memory communication, in-memory processing allows the computations to be performed on the memory chip thus reducing the processor-memory performance gap. In-memory processing provides an attractive optimization for IoT devices with massive amounts of data generated and resources constraints of IoT devices. From edge computing point of view, in-memory processing offers real-time in-situ data processing on large data amounts. In order to achieve energy-efficient data processing and low hardware overhead, inherently robust brain-inspired models are explored [9]. The compute sensor is another architecture and similar to the computer memory and provides in-sensor processing which high potential for IoT devices [39]. With compute sensor, sensor-processor interface is eliminated and the sensed data is transmitted to the processor for visualization. Both latency and energy consumption are reduced when using the compute sensor [39]. Both memory and sensor computes offer new optimization aspects for IoT devices.

2.6 Secure Microarchitecture Paradigm

Some of the most important applications that will be executed on IoT microprocessors are security applications. IoT devices resources constraints make security a challenging as they will not have hardware support for enhance security features [40]. In addition to resources constraints, IoT devices may generate sensitive information [41]. Most of hardware security techniques that proposed for embedded systems [10] [42-44] can be used in IoT devices with runtime configurable security policies which adaptable to the requirements [11]. Multiple optimization goals can be achieved, and runtime time configurability is easily augmented with security at the level of microarchitecture. However, the security at the level of microarchitecture should not be at the expense of energy consumption or any other optimization goals.

3 Proposed Microarchitecture with Reconfigurable Pipeline Stages

The fixed microarchitecture based microprocessor as a core for any development is considered as a drawback for its utilization with the-state-of-the-art IoT technology. When the user is going to use the development at the IoT edge-level, the same amount of power consumption is required regardless the application frequency requirements and hence the need of the proposed microarchitecture is necessary for reduction of the consumed power from one side and ensuring accurate frequency measurement from another side. The proposed microarchitecture diagram is shown in figure 4 illustrating the passing of sensor pulses through different parts. The proposed computing system uses reconfigurable pipeline stages according to the frequency of incoming pulses from an external sensor.

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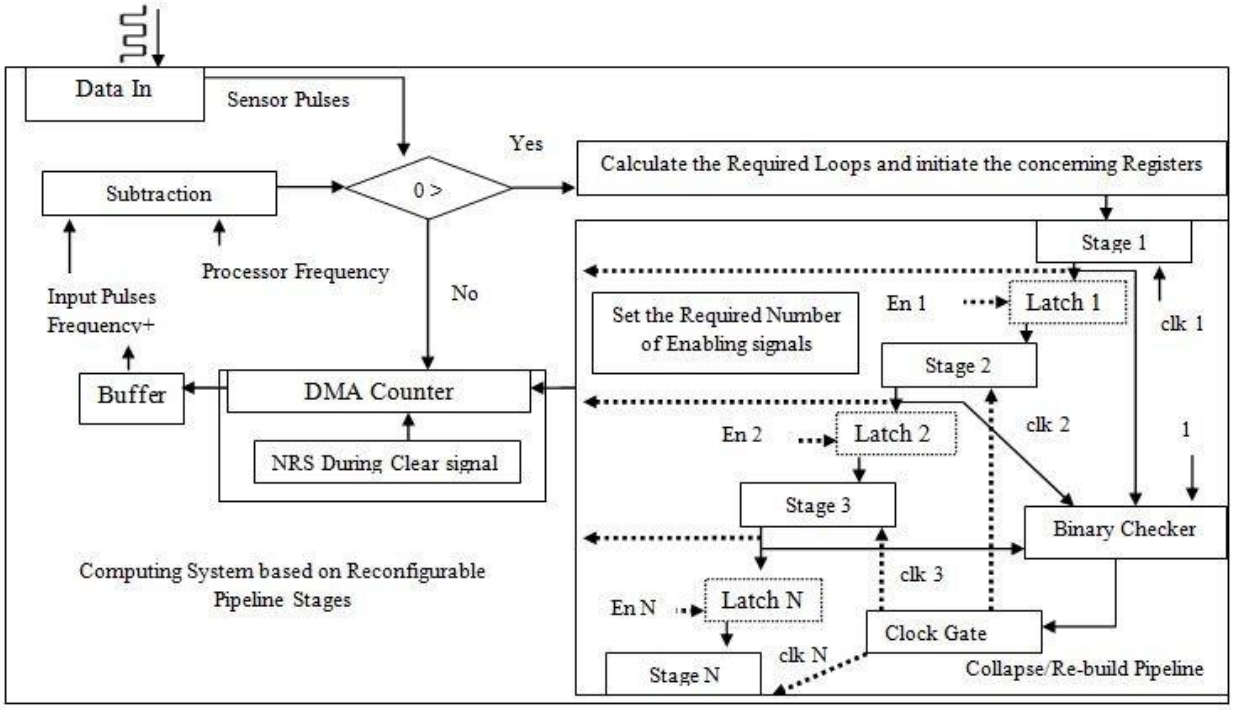

Figure 2: Proposed Microarchitecture for the IoT-Edge Computing.

However, if the mentioned frequency is found to be larger than the processor frequency then the required loops (pipeline stages) are calculated and the concerning registers are initiated. A binary checker (through which the required clock signals are delivered [45]) is employed to ensure the pulses propagation from one stage to the other with the help of enabling signals eliminating the pulses overlaps. A direct memory access (DMA) counter can be used to determine the pulses frequency and it's not ready sequence (NRS) due to the clear signal is avoided because of current mechanism delay time for collapse/re-build loops. In addition to that, the DMA method is found to be the best for frequency measurement, but it has the problems of NRS and data propagation delay which can be solved via pipeline system, but with fixed processor architecture the pipeline stages number is fixed which a drawback, and therefore this can be solved via dynamic (reconfigurable) microarchitecture. The proposed microarchitecture benefits in the IoT domain are reduction of the power consumption and resource utilization especially at the edge-level of the IoT architecture to which sensors producing pulses are connected. The edge computing can be performed with the help of this proposed reconfigurable microarchitecture so that the number of the initiated loops will dependent on the input pulses frequency and hence the consumed power and the utilized microarchitecture resources. However, when the proposed microarchitecture scheme is implemented at the IoT - edge level delay problems is avoided, and the necessary computations are done in Edge level letting both Gateway and Cloud levels for the task of data of interest transmission, receiving, visualize and analysis.

4 Conclusion

In this manuscript, the paradigms of the microarchitecture optimization are reviewed. Adaptable/configurable architectures, distributed heterogeneous architectures, energy harvesting and nonvolatile processors, approximate computing, in-memory processing and secure microarchitecture are the key paradigms which to be considered for the microarchitecture optimization in the IoT domain. In addition to that, we introduced a proposed reconfigurable computing system based on collapsing/re-building pipeline stages for the aim of insuring efficient power consumption and resource utilization while performing the computations at the IoT-edge level. Incoming pulses frequency determines the microarchitecture pipeline stages and hence its power consumption and resource utilization which considered as an acceptable solution at the IoT edge level. Employing the suggested microarchitecture design in an industrial application, testing its performance, and proofing the utilization of it in the IIoT domain are the goals of our future research activities.

Conflicts of Interest Statement

The authors certify that they have NO affiliations with or involvement in any organization or entity with any financial interest (such as honoraria; educational grants; participation in speakers' bureaus; membership, employment, consultancies, stock ownership, or other equity interest; and expert testimony or patent-licensing arrangements), or non-financial interest (such as personal or professional relationships, affiliations, knowledge or beliefs) in the subject matter or materials discussed in this manuscript.

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